DHANALAKSHMI SRINIVASAN ENGINEERING COLLEGE
(AUTONOMOUS)
(Approved by AICTE & Affiliated to Anna University, Chennai)
Re-Accredited with 'A' Grade by NAAC, Accredited by TCS
Accredited by NBA – BME, ECE & EEE
PERAMBALUR - 621 212. Tamil Nadu.
website : www.dsengg.ac.in

COURSE PLAN

Name of the Faculty				
Designation/Department	AP/IT			
Course Code/Name	U23ITT31 / COMPUTER ORGANIZATION AND ARCHITECTURE			
Year/Section/Department	II/C /IT			
Credits Details	L: 3	T: 0	P: 0	C: 3
Total Contact Hours Required	45			

Syllabus:

UNIT I/ OVERVIEW & INSTRUCTIONS	**No. Of Periods: 9**
Eight ideas - Components of a computer system - Technology - Performance - Power wall - Uniprocessors to multiprocessors; Instructions - operations and operands - representing instructions - Logical operations - control operations - Addressing and addressing modes	
UNIT II/ ARITHMETIC OPERATIONS	**No. Of Periods: 9**
ALU - Addition and subtraction - Multiplication - Division - Floating Point operations - Sub word Parallelism.	
UNIT III/ PROCESSOR AND CONTROL UNIT	**No. Of Periods: 9**
Basic MIPS implementation - Building data path - Control Implementation scheme - Pipelining - Pipelined data path and control - Handling Data hazards & Control hazards – Exceptions.	
UNIT IV/ PARALLELISM	**No. Of Periods: 9**
Instruction-level-parallelism - Parallel processing challenges - Flynn's classification - Hardware multithreading - Multicore processors	
UNIT V/ MEMORY AND I/O SYSTEMS	**No. Of Periods: 9**
Memory hierarchy – Memory technologies – Cache basics – Measuring and improving cache performance – Virtual memory, TLBs – Input/output system, programmed I/O, DMA and interrupts, I/O processors.	

Objective:

- To make students understand the basic structure and operation of digital computer.
- To understand the hardware – software interface.
- To familiarize the students with arithmetic and logic unit and implementation of fixed point and floating – point arithmetic operations.
- To familiarize the students with hierarchical memory system including cache memories and Virtual memory.

Text Books:

T1: David A. Patterson and John L. Hennessey, "Computer organization and design", Morgan Kauffman Elsevier, Fifth edition, 2014.

T2: Structured Computer Organization, Andrew S.Tanenbaum "Structured Computer Organization" sixth Edition 2021.

Reference Books:

R1: Carl Hamacher. V, Zvonko G. Varanesic and Safat G. Zaky, "Computer Organization", 6th edition, Mc Graw-Hill Inc, 2012.

R2: William Stallings "Computer Organization and Architecture", 11th Edition, Pearson Education, 2006.

R3: Vincent P. Heuring, Harry F. Jordan, "Computer System Architecture", 2nd Edition, Pearson Education, 2005.

R4: Govindarajalu, "Computer Architecture and Organization, Design Principles and Applications", 1st edition, Tata McGraw Hill, New Delhi, 2005.

Website:

W1: https://www.tutorialspoint.com/computer_organization/index.asp

W2: https://www.gatevidyalay.com/addressing-modes/

W3: https://www.geeksforgeeks.org/computer-organization-performance-of-computer

W4: https://edurev.in/studytube/Sub-Word-Parallelism-Arithmetic-Operations

Online Mode of Study:

W1: https://onlinecourses.nptel.ac.in/noc24_cs83/preview

W2: https://onlinecourses.swayam2.ac.in/cec24_cs10/preview

W3: https://onlinecourses.nptel.ac.in/noc24_cs93/preview

Course Plan:

Topic Number	Topic	Reference Detail	Page Number	Mode of teaching	Number of Periods Required	Cumulative Period
UNIT I - OVERVIEW & INSTRUCTIONS						
1	Eight Ideas	T1		BB	1	1
2	Components of a Computer System, Technology	T1	10 – 26	BB	1	2
3	Performance	T1, W1	26 – 36	BB	1	3
4	Power Wall, Uniprocessors to Multiprocessors	T1	39 – 44	BB	1	4
5	Instructions	T1, R1	105 – 111	BB	1	5
6	Operations and Operands	T1	77 – 80	BB	1	6
7	Representing Instructions	T1	93 – 100	PPT	1	7
8	Logical Operations, Control Operations	T1	100 – 105	BB	2	9
9	Addressing and Addressing Modes	T1	127 -133	BB	2	11
Outcome of Unit I: **CO1:** Understand the basic components of computers, operations and instructions.						
UNIT II - ARITHMETIC OPERATIONS						
10	ALU, Addition and Subtraction	T1, R1	178-182	BB	2	13
11	Multiplication	T1	183-188	PPT	2	15
12	Division	T1	189-195	BB	3	18
13	Floating Point Representation	T1	196-202	BB	1	19
14	Floating Point Operations	T1	203-208	PPT	1	20
15	Sub word Parallelism	T1, W2	56-59	BB	1	21
Outcome of Unit II: **CO2:** Explain the design concepts of arithmetic and logic unit						

UNIT III - PROCESSOR AND CONTROL UNIT						
16	A Basic MIPS implementation	T1	244-250	BB	1	22
17	Building a Data path	T1	250-258	BB	1	23
18	Control Implementation Scheme	T1	259-271	PPT	1	24
19	Pipelining	T1, R2	272-280	BB	1	25
20	Pipelined data path and control	T1, W3	330 - 348	BB	2	27
21	Handling Data Hazards	T1, R2	303-312	PPT	1	28
22	Handling Control Hazards	T1, R2	316-324	BB	2	30
23	Exceptions	T1	324-325	BB	1	31
Outcome of Unit III: **CO3:** Apply pipelined control units and the different types of hazards in the instructions						
UNIT IV - PARALLELISM						
24	Instruction-level-parallelism	T1, W4	212	PPT	1	32
25	Parallel processing challenges	T1	5 - 10	BB	2	34
26	Flynn's classification	T1	509 - 511	BB	1	35
27	Hardware multithreading	T1	444 - 449	PPT	2	37
28	Multicore processors	T1, W4	519 - 523	BB	2	39
Outcome of Unit IV: **CO4:** Interpret the concepts of parallel processing architectures						
UNIT V - MEMORY AND I/O SYSTEMS						
29	Memory hierarchy	T1, W4	519-523	PPT	1	40
30	Memory technologies	T1	288-289	PPT	1	41
31	Cache basics, Measuring and improving cache performance	T1	289-310	BB	2	43
32	Virtual memory	T2	404- 428	PPT	1	44
33	TLBs	R2	325 - 328	BB	1	46

34	Input/Output System, Programmed I/O	R2	259 – 359	BB	1	47
35	DMA and Interrupts	R2	263 – 278	PPT	1	48
36	I/O Processors	R2	285 – 287	PPT	2	50

Outcome of Unit V:
CO5: Summarize the fundamentals of memory system
CO6: Explain the concepts of I/O System

Course Outcome:

At the end of course: Students should be able to do:
- **CO1:** Understand the basics structure of computers, operations and instructions
- **CO2:** Explain the design concepts of arithmetic and logic unit
- **CO3:** Apply pipelined control units and the different types of hazards in the instructions
- **CO4:** Interpret the concepts of parallel processing architectures
- **CO5:** Summarize the fundamentals of memory system
- **CO6:** Explain the concepts of I/O system

Course Outcome Vs Program Outcome Mapping:

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	1	-	-	-	-	-	-	-	-	-	-
CO2	3	3	1	2	-	-	-	-	-	-	-	-	-	-
CO3	3	2	1	2	-	-	-	-	-	-	-	-	-	-
CO4	3	2	2	2	-	-	-	-	-	-	-	-	-	-
CO5	3	3	1	1	-	-	-	-	-	-	-	-	-	-
CO6	2	2	1	2	-	-	-	-	-	-	-	-	-	-
AVG	2.83	2.5	1.33	1.67	-	-	-	-	-	-	-	-	-	-

Content beyond Syllabus:

- ❖ RISC and CISC in Computer Organization.
- ❖ IEEE Number Standards.

Internal Evaluation Components:

Webportal	Assignment	Components	Topic Number with Topic / Unit Details	Relevance to CO
Webportal 1	--	Assessment – I (60)	Unit I and II	CO1 & CO2
	1	Handwritten (20)	1. Eight Ideas 2. Components of a computer system 8. Logical operations, Control operations 9. Addressing and addressing modes	CO1
	2	Poster Presentation / PPT (20)	10. Addition and Subtraction 11. Multiplication 12. Division 14. Floating Point Operations	CO2
Webportal 2	--	Assessment – II (60)	Unit III and IV	CO3 & CO4
	3	Seminar (20)	19. Pipelining 20. Pipelined data path and control 21. Handling Data hazards 22. Control hazards	CO3
	4	Case Study Report (20)	26. Flynn's classification 27. Hardware multithreading 38. TLBs 41. DMA and interrupts	CO4 & CO5
Webportal 3	--	Model Exam (75)	Unit I to V	CO1 to CO6
	5	MCQ (15)	Unit I to V	CO1 to CO6
	-	Course Attendance (10)	--	--

Submission Details:

Phase 1(Before AT 1)		Phase 2 (Before AT 2)		Phase 3 (Model)
Assignment 1	Assignment 2	Assignment 3	Assignment 4	Assignment 5

Google Class Code Details:

Class Name: U23ITT31 - COMPUTER ORGANIZATION AND ARCHITECTURE

PLAN OF ASSESSMENT TEST –DISTRIBUTION OF MARKS:

TEST	CO- MARK WISE DISTRIBUTION						BLOOM'S LEVEL MARK WISE DISTRIBUTION					
AT-1	CO1	CO2	CO3	CO4	CO5	CO6	BTL1	BTL2	BTL3	BTL4	BTL5	BTL6
	37	23	-	-	-	-	18	29	13	-	-	-
AT-2	CO1	CO2	CO3	CO4	CO5	CO6	BTL1	BTL2	BTL3	BTL4	BTL5	BTL6
MODEL	CO1	CO2	CO3	CO4	CO5	CO6	BTL1	BTL2	BTL3	BTL4	BTL5	BTL6

Prepared By

Verified By
HOD/IT

Approved By
Principal